WHAT IS CLAIMED IS

1. A processor comprising:

a plurality of functional units, including a multiplier unit and an arithmetic logic

unit, to execute operations defined from an instruction set of the processor, wherein

each of the plurality of functional units has an output that can be explicitly referenced in

instructions defined from the instruction set.

2. A processor as recited in claim 1, further comprising:

a plurality of dedicated output buses, one for each of the functional units; and

a plurality of bus registers, each coupled to store the output of only a

corresponding one of the plurality of functional units and each coupled to only a

corresponding one of the plurality of dedicated output buses.

3. A processor as recited in claim 2, wherein each of the dedicated output buses is

coupled to an input of at least one other of the plurality of functional units.

4. A processor as recited in claim 1, wherein the instruction set has a hierarchy of

instruction levels, each of which can be used by a programmer to define instructions for

the processor, the hierarchy of instruction levels including:

a RISC/CISC assembly code level; and

a free pipeline assembly code level.

5. A processor as recited in claim 4, wherein the free pipeline assembly code level

comprises a native machine language of the processor.

6. A processor as recited in claim 4, wherein the plurality of hierarchical instruction levels further include a vector processing assembly code level.

7. A processor as recited in claim 6, further comprising a plurality of special use control registers, wherein the plurality of hierarchical instruction levels further comprise a level for using the special use control registers.

8. A processor comprising:

a multiplier unit adjustable to multiply integer data words of any of a plurality of different lengths in response to instructions defined in an instruction set of the processor, the plurality of different lengths being integer multiples of each other, wherein the instruction set has a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor;

an arithmetic logic unit (ALU) adjustable to perform arithmetic operations on integer data words of any of the plurality of different lengths in response to instructions defined in the instruction set;

a shift register to perform shift operations in response to instructions defined in the instruction set;

a plurality of dedicated output buses, one for each of the multiplier unit, the ALU, and the shift register; and

a plurality of bus registers, each coupled to an output of a separate corresponding one of the multiplier unit, the ALU, and the shift register and to a separate corresponding one of the plurality of dedicated output buses, the bus registers to hold outputs of the multiplier unit, the ALU, and the shift register, respectively,

16

wherein the outputs of the multiplier unit, the ALU, and the shift register can be explicitly referenced by instructions defined from the instruction set.

9. A processor as recited in claim 8, wherein the hierarchy of instruction levels includes:

    a RISC/CISC assembly code level;

    a free pipeline assembly code level; and

    a vector processing assembly code level.

10. A processor as recited in claim 9, wherein the free pipeline assembly code level comprises a native machine language of the processor.

11. A processor as recited in claim 9, further comprising a plurality of special use control registers, wherein the plurality of hierarchical instruction levels further comprise a level for using the special use control registers.

12. A processor as recited in claim 8, wherein the ALU has at least three operand inputs, further comprising:

    a control register containing a plurality of bits which define a three port parametrised logic function to be performed on the at least three operand inputs, the ALU receiving a plurality of bits from the control register to execute the three port parametrised logic function.